

1200V, 30mΩ, TO-247-4L SiC MOSFET

Features

- Low On-Resistance and High Current Density
- Low Capacitance for High Frequency Operation
- Positive Temperature Coefficient Device
- Low impedance Kelvin source pin-out
- AEC-Q101 Qualified
- RoHS Compliant and Halogen Free

Benefits

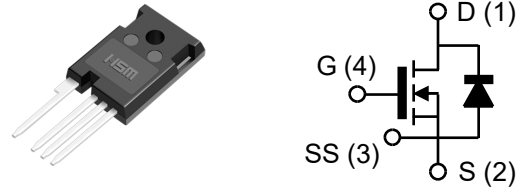
- Higher System Efficiency
- Increase Parallel Device Convenience
- Capable of 175°C High T_j Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems

Applications

- Switching Mode Power Supply
- DC/DC Converters, UPS, and PFC
- EV Charging Station
- Motor Drives
- Power Inverters
- Solar/Wind Renewable Energy

V_{DS}	1200V
$I_D(@25^{\circ}C)$	78 A
$R_{DS(on)}$	30mΩ

Circuit Diagram



Description

The H1M30120K 1200V, 30mΩ silicon carbide power MOSFET is an N-channel enhancement mode device. Exploiting the outstanding wide bandgap material properties, this device shows high current density and great switching behavior. Thanks for the excellent thermal conductivity and many advantages of SiC, this device significantly improved in thermal capability and temperature independent switching behavior. With the high stability and reliability, this device also passes the qualification criteria based on AEC-Q101.

Absolute Maximum Ratings ($T_c = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS,max}$	$V_{GS}=0V, I_{DS}=100\mu A$	1200	V
Continuous Drain Current	I_D	$V_{GS}=20V, T_c=25^{\circ}C$	78	A
		$V_{GS}=20V, T_c=110^{\circ}C$	53	
Pulse Drain Current	$I_{D,pulse}$	t_{PW} limitation per Fig.15	349	
Avalanche energy, Single Pulse	E_{AS}	$V_{DD}=100V, I_D=14A$	2500	mJ
Power Dissipation	P_D	$T_c=25^{\circ}C$	375	W
Recommend Gate Source Voltage	$V_{GS,op}$	Static, recommended DC operating values	-5 to 20	V
Maximum Gate Source Voltage	$V_{GS,max}$	Transient operating limit (AC f > 1Hz, duty cycle < 1%)	-10 to 25	
Junction & Storage Temperature	T_j, T_{stg}		-55 to 175	$^{\circ}C$
Soldering Temperature	T_L		260	
Mounting Torque	M_D	M3 or 6-32 screw	1.0	Nm

Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		0.4		$^{\circ}C/W$

Electrical Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _{DS} =100μA	1200			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =10V, I _{DS} =50mA		2.7		V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =1200V, V _{GS} =0V		<1	50	μA
		V _{DS} =1200V, V _{GS} =0V T _j =175°C		10	500	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =20V, V _{DS} =0V			250	nA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =20V, I _{DS} =40A		30	40	mΩ
		V _{GS} =20V, I _{DS} =40A, T _j =175°C		54		
Transconductance	g _{fs}	V _{DS} =15V, I _{DS} =40A		17		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =800V f=1MHz, V _{AC} =25mV		4909		pF
Output Capacitance	C _{oss}			198		
Reverse Transfer Capacitance	C _{rss}			34		
Effective Output Capacitance, Energy Related	C _{o(er)}	V _{GS} =0V, V _{DS} =0 to 800V		257		
Effective Output Capacitance, Time Related	C _{o(tr)}	I _D =const., V _{GS} =0V, V _{DS} =0 to 800V		359		
Turn On Delay Time	t _{d(on)}	V _{DS} =800V, V _{GS} =-4/+20V, I _D =40A, R _L =20Ω, R _{G(ext)} = 2.7 Ω		31		ns
Rise Time	t _r			55		
Turn Off Delay Time	t _{d(off)}			8		
Fall Time	t _f			12		
C _{oss} Stored Energy	E _{oss}	V _{GS} =0V, V _{DS} =800V f=1MHz, V _{AC} =25mV		80.5		μJ
Turn-on Switching Energy	E _{on}	V _{DS} =800V, V _{GS} =0/20V, I _D =40A,		167*		
Turn-off Switching Energy	E _{off}	R _{G(ext)} = 2.7 Ω		254*		
Internal Gate Resistance	R _{G(int.)}	f=1MHz, V _{AC} =25mV		0.7		Ω

*Based on the results of calculation, note that the energy loss caused by the reverse recovery of free-wheeling diode is not included in E_{on}.

Built-in SiC Diode Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _{SD} =10A	3.0	V
Continuous Diode Forward Current	I _S	V _{GS} =0V, T _c =25°C	50	A
Reverse Recovery Time	t _{rr}	V _{GS} =0V,	79	ns
Reverse Recovery Charge	Q _{rr}	I _{SD} =30A, V _{DS} =400V, di/dt=300A/μs	284	nC
Peak Reverse Recovery Current	I _{rrm}		6.8	A

Gate Charge Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q _{GS}	V _{DS} =800V, V _{GS} =-5/+20V, I _D =40A	91	nC
Gate to Drain Charge	Q _{GD}		88	
Total Gate Charge	Q _G		305	
Gate plateau voltage	V _{pl}		7.9	V

Typical Device Performance

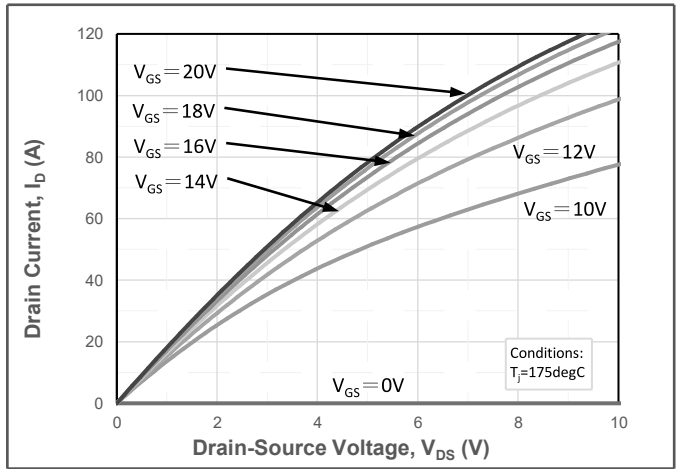
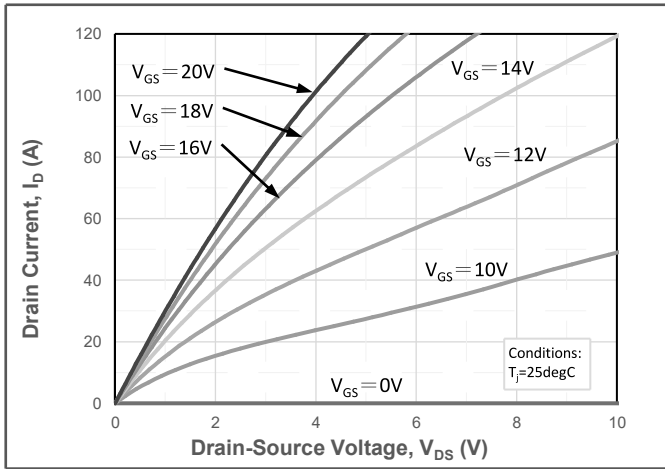


Fig.1 Forward Output Characteristics at $T_j = 25^\circ\text{C}$

Fig.2 Forward Output Characteristics at $T_j = 175^\circ\text{C}$

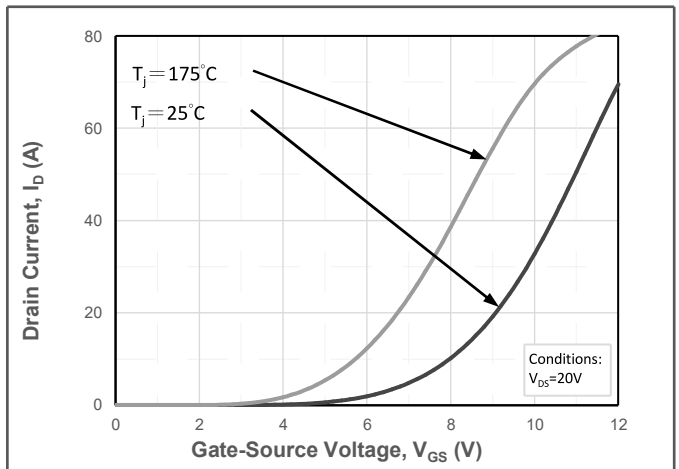
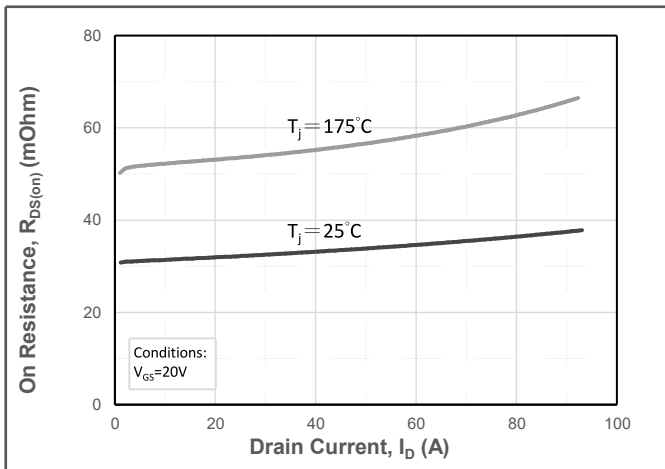


Fig.3 On-Resistance vs. Drain Current for Various T_j

Fig.4 Transfer Characteristics for Various T_j

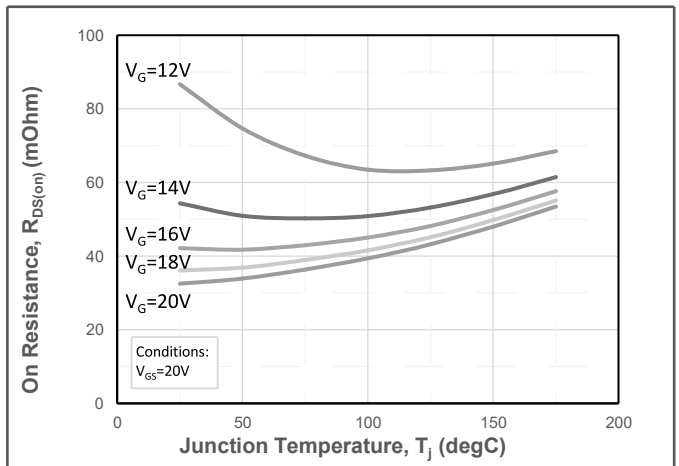
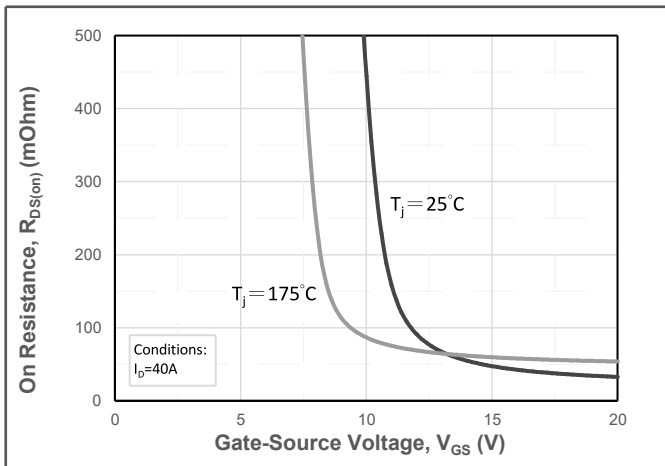


Fig.5 On-Resistance vs. Gate Voltage for Various T_j

Fig.6 On-Resistance vs. Temperature for Various Gate Voltage

Typical Device Performance

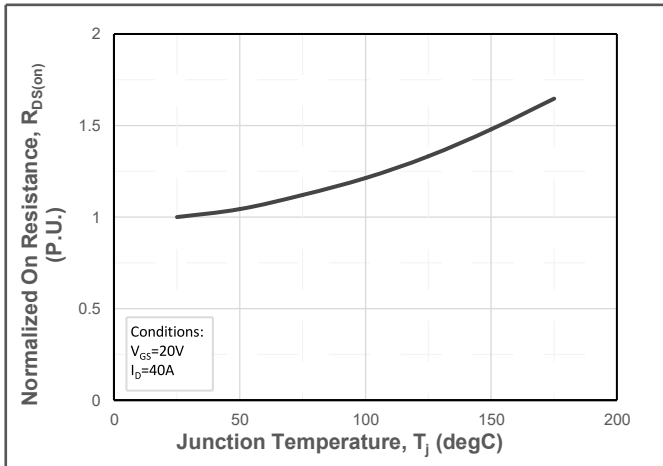


Fig.7 Normalized On-Resistance vs. Temperature

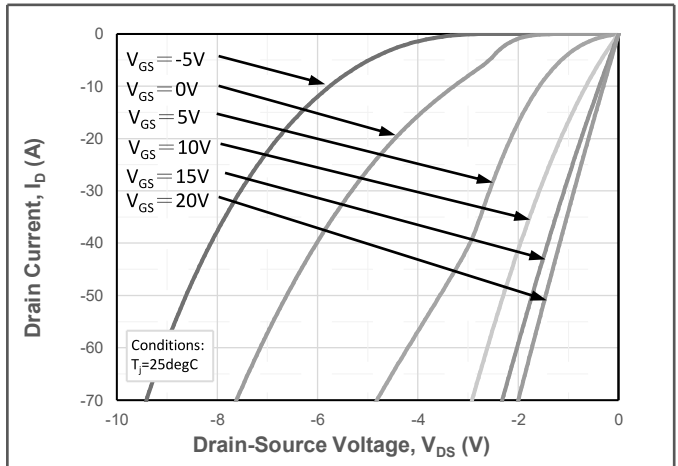


Fig.8 Reverse Output Characteristics at $T_j = 25^\circ C$

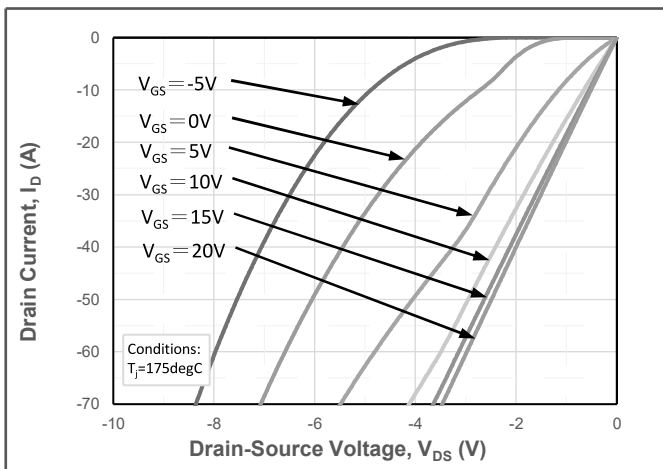


Fig.9 Reverse Output Characteristics at $T_j = 175^\circ C$

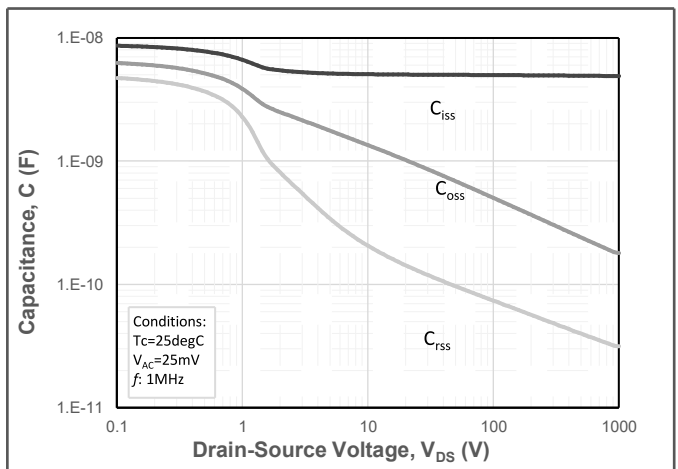


Fig.10 Capacitances vs. Drain to Source Voltage

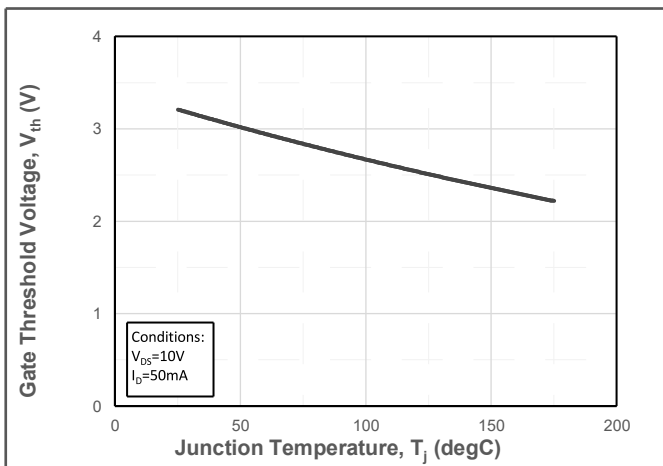


Fig.11 Threshold Voltage vs. Temperature

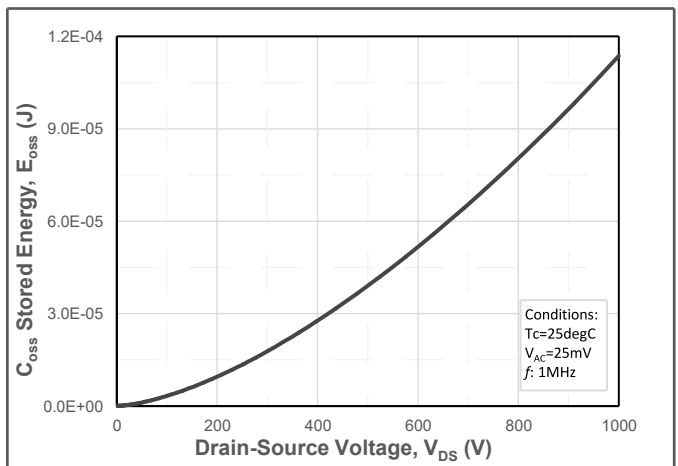


Fig.12 Output Capacitor Stored Energy

Typical Device Performance

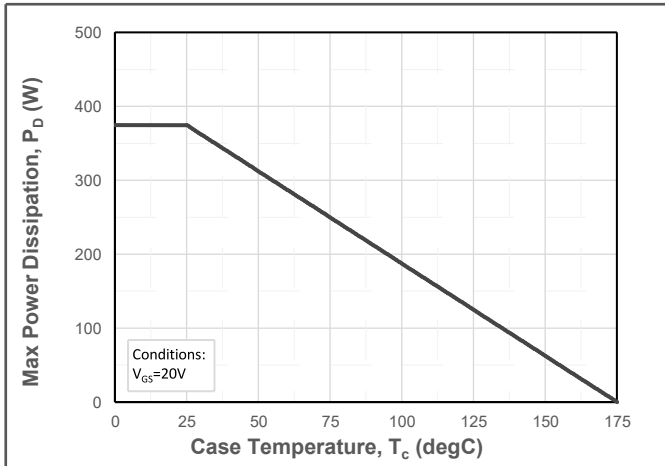


Fig.13 Maximum Power Dissipation Derating vs. Case Temperature

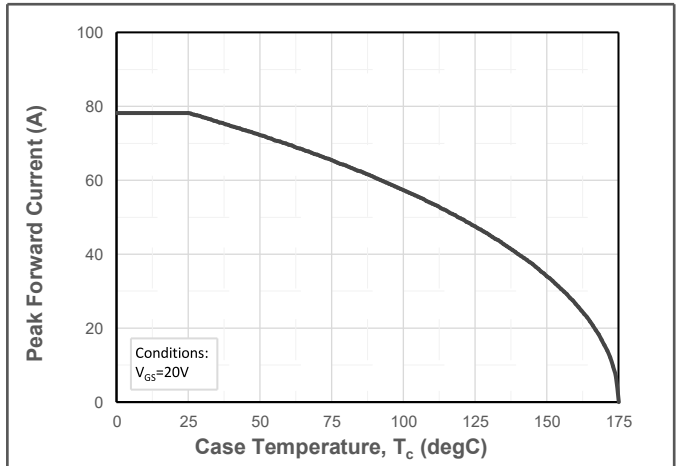


Fig.14 Drain Current Derating vs. Case Temperature

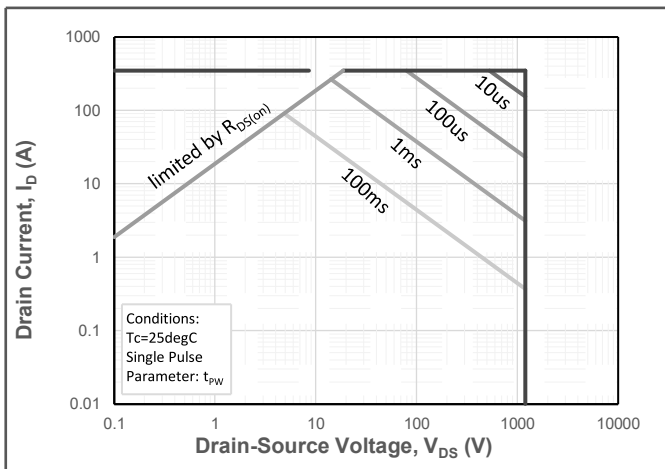


Fig.15 Safe Operating Area

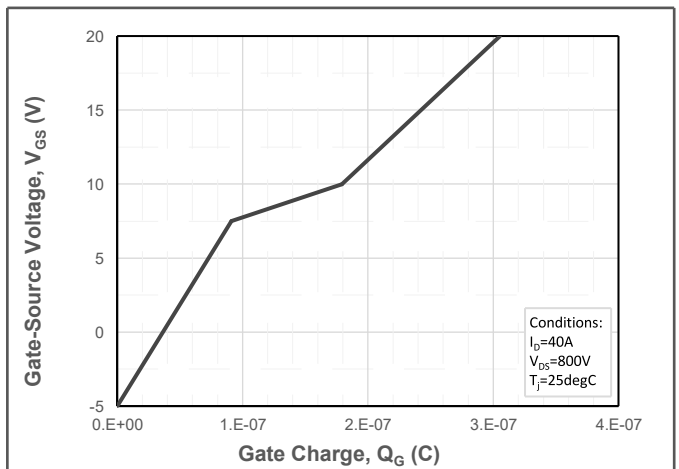


Fig.16 Gate Charge Characteristics

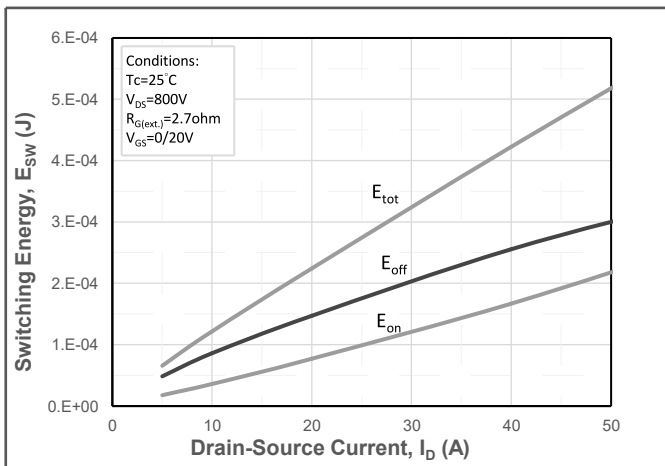


Fig.17 Clamped Inductive Switching Energy vs. Drain Current

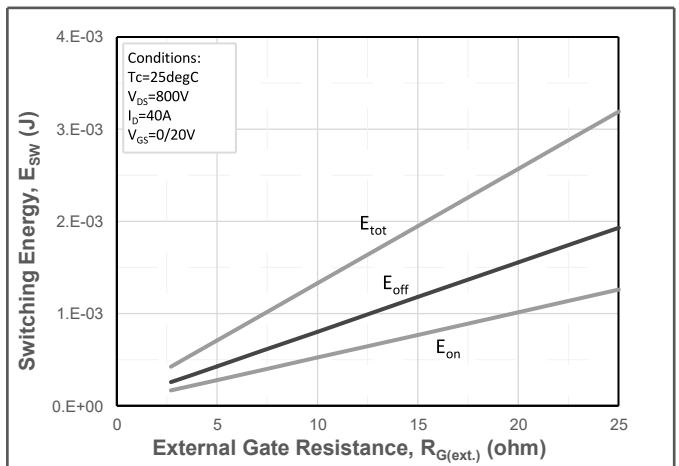


Fig.18 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)

Typical Device Performance

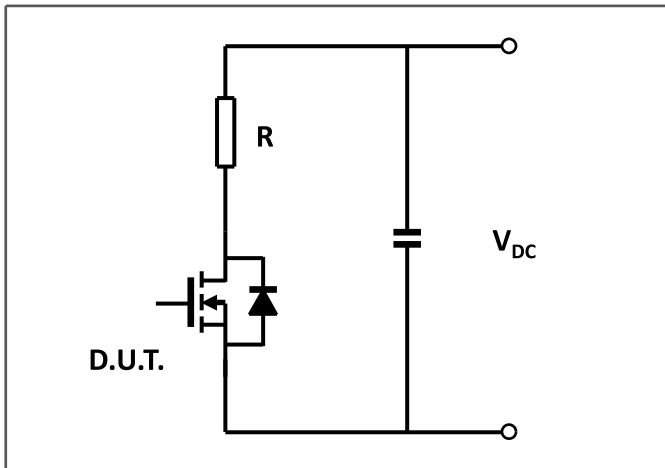


Fig.19 Schematic of Resistive Switching

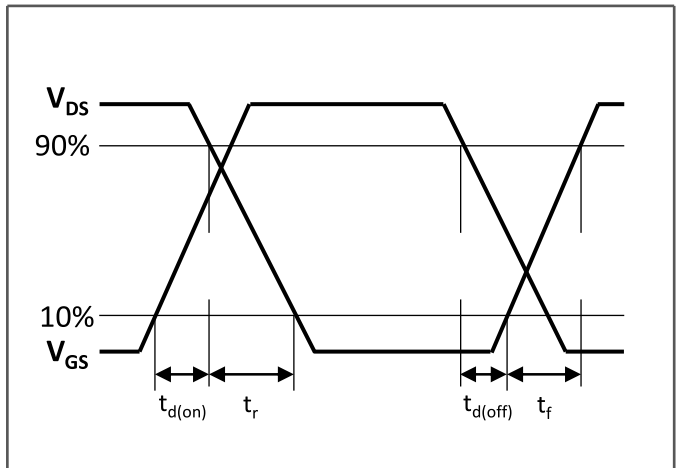


Fig.20 Switching Times Definition

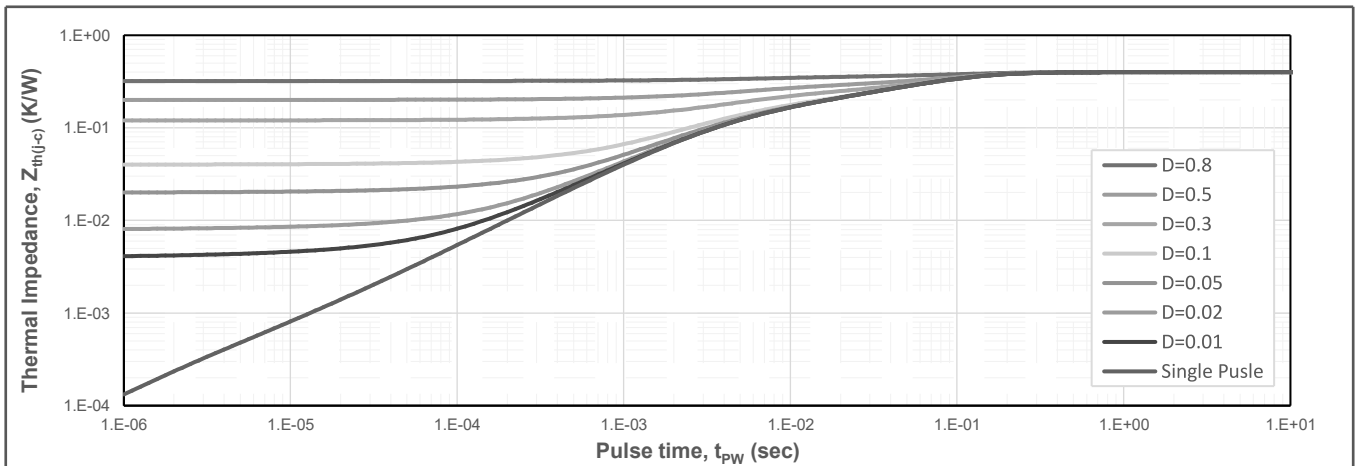
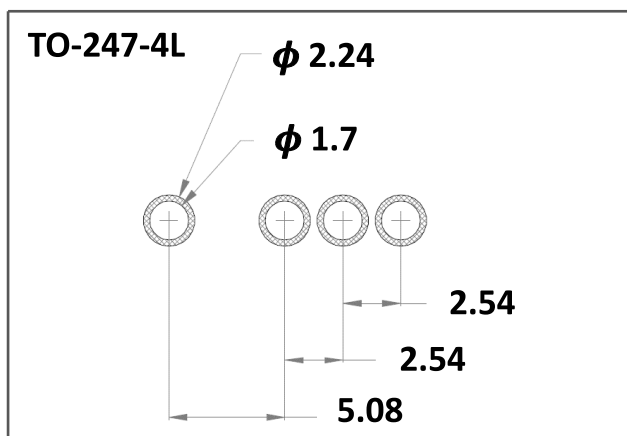
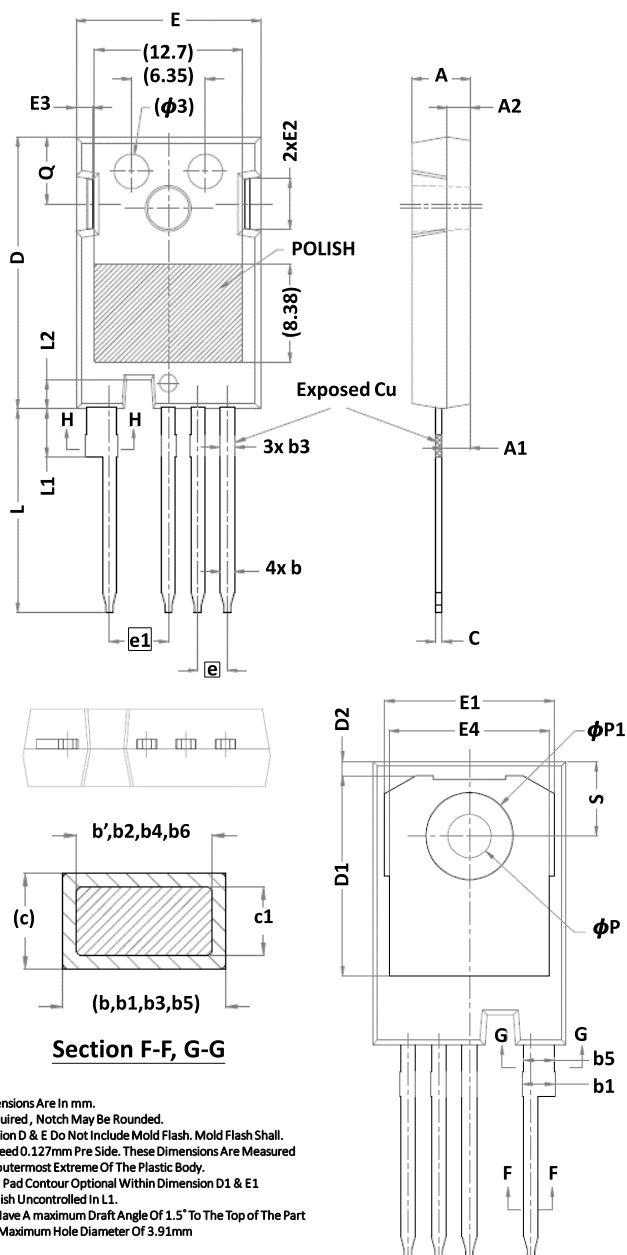


Fig.21 Transient Junction to Case Thermal Impedance

Recommended Solder Pad Layout



Package Dimensions



Note:

1. All Dimensions Are In mm.
2. Slot Required, Notch May Be Rounded.
3. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Per Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
4. Thermal Pad Contour Optional Within Dimension D1 & E1
5. Lead Finish Uncontrolled In L1.
6. ϕP To Have A maximum Draft Angle Of 1.5° To The Top Of The Part With A Maximum Hole Diameter Of 3.91mm

Symbol	mm		
	Min.	Typ.	Max.
A	4.83	5.02	5.21
A1	2.29	2.41	2.54
A2	1.91	2.00	2.16
b'	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b2	2.39	2.67	2.84
b3	1.07	1.30	1.60
b4	1.07	1.30	1.50
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54 BSC		
e1	5.08 BSC		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
ϕP	3.51	3.61	3.65
$\phi P1$	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

Notes

- The information provided herein is subject to change without notice.
- For other information that does not show on this datasheet, please contact us for inquiry.