HMM**100N50**

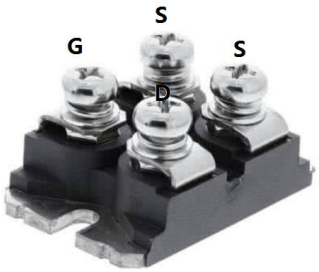
Silicon N-Channel Power MOSFET

V_{DSS}	500	V
I_D	94	A
$P_D(T_C=25℃)$	780	W
$R_{DS(ON)TYP}$	42	mΩ

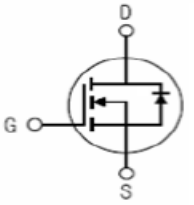
General Description :

HMM100N50 the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned Super-junction Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is SOT-227B, which accords with the RoHS standard.

SOT-227B



Inner Equivalent Principium Chart



Features :

- Fast Switching
- Low Gate Charge and R_{dson}
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications :

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)

Absolute（Tc=25℃ unless otherwise specified）:

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current	94	A
I_{DM}[a1]	Pulsed Drain Current (Pulse Width Limited by T_{JM})	240	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	3.5	J
P_D	Power Dissipation	780	W
T_J , T_{stg}	Operating Junction and Storage Temperature Range	150 , −55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	0.16	℃/W

Electrical Characteristics (Tc=25℃ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	500	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=500V,V_{GS}=0V,T_a= 25℃	--	--	10	μA
		V_{DS}=400V,V_{GS}=0V,T_a=150℃	--	--	1000	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$[a3]	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=20A	--	42	55	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.5	--	4.5	V

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}[a3]	Forward Transconductance	V_{DS}=10V, I_D=47A	--	58	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_D=50V f=1.0MHz	--	16000	--	pF
C_{oss}	Output Capacitance		--	1410	--	
C_{rss}	Reverse Transfer Capacitance		--	120	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=400V,I_D=47A, V_{GS}=10V R_g=1.7Ω	--	68	--	ns
t_r	Rise Time		--	120	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	500	--	
t_f	Fall Time		--	150	--	
Q_g	Total Gate Charge	I_D =40A,V_{DD}=500V V_{GS}=0 to 10V	--	280	--	nC
Q_{gs}	Gate to Source Charge		--	44	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	96	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	94	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	240	A
V_{SD}	Diode Forward Voltage	I_S=68A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_R=500V, V_{GS}=0V	--	600	--	ns
Q_{rr}	Reverse Recovery Charge	I_S=I_F,d_i/d_t=100A/us	--	3.5	--	uC
Pulse width tp≤380μs,δ≤2%						

[a1] : Repetitive rating; pulse width limited by maximum junction temperature
[a2] : I_{AS}=94A,V_{DD}=50V,R_G=25Ω, Starting T_J= 25°C
[a3] : Pulse Test: Pulse width≤380us, Duty Cycle≤2%

Fig. 1. Output Characteristics @ T_J = 25°C

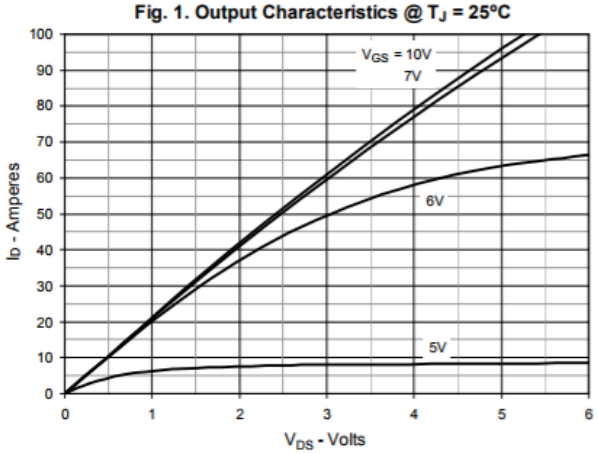


Fig. 2. Extended Output Characteristics @ T_J = 25°C

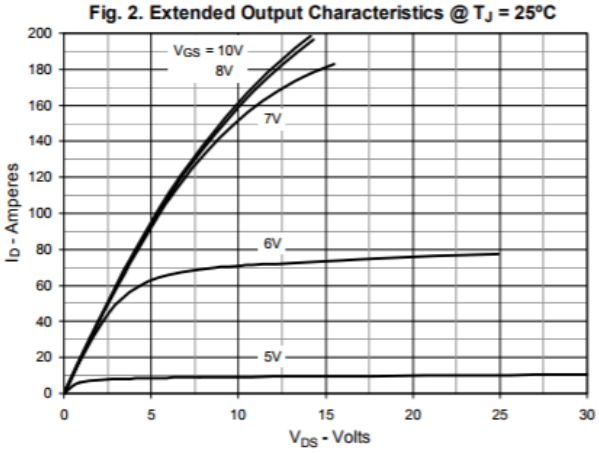


Fig. 3. Output Characteristics @ T_J = 125°C

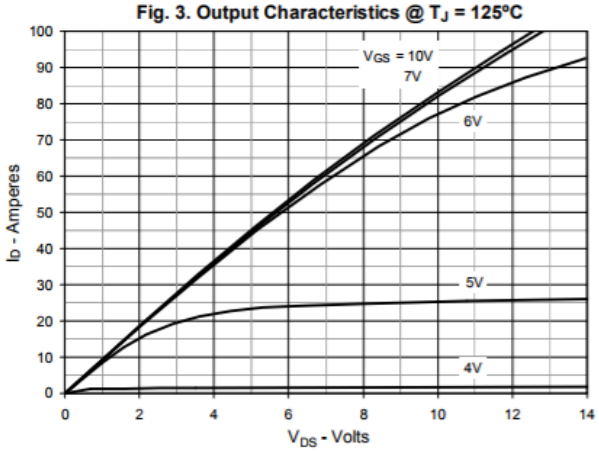


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 47A Value vs. Junction Temperature

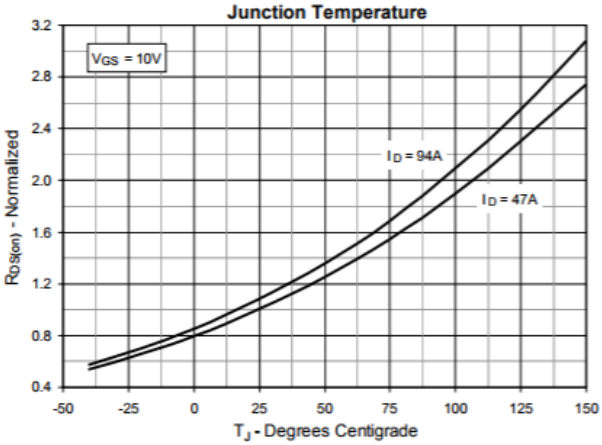


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 47A Value vs. Drain Current

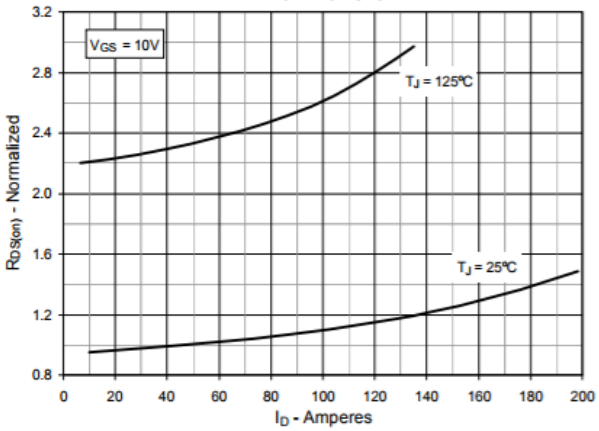


Fig. 6. Maximum Drain Current vs. Case Temperature

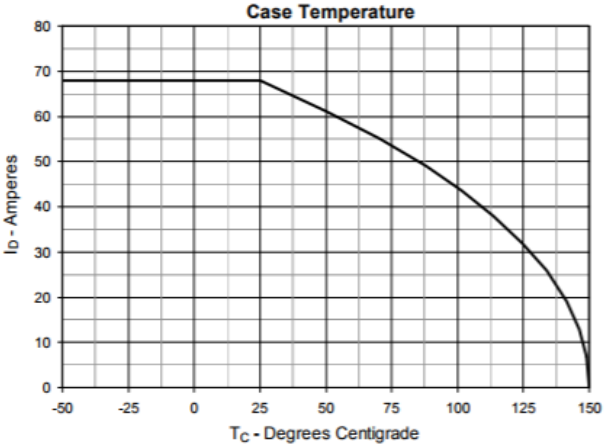


Fig. 7. Input Admittance

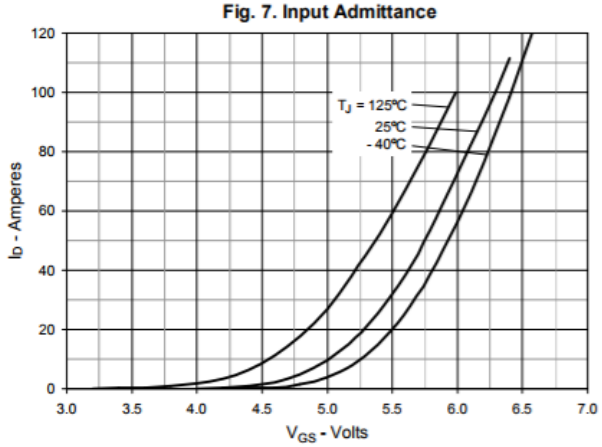


Fig. 8. Transconductance

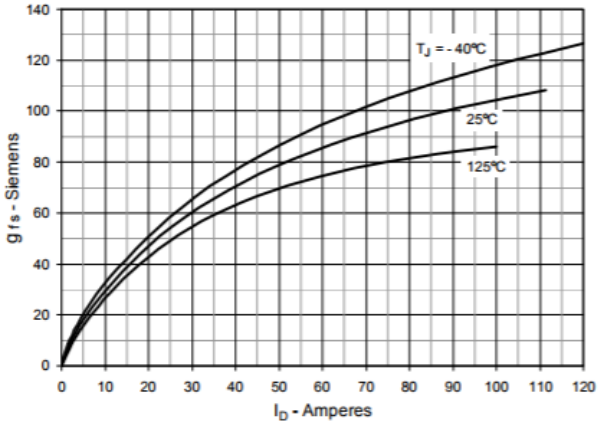


Fig. 9. Forward Voltage Drop of Intrinsic Diode

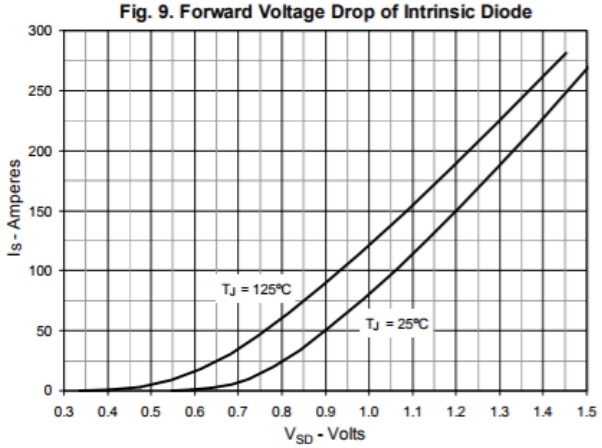


Fig. 10. Gate Charge

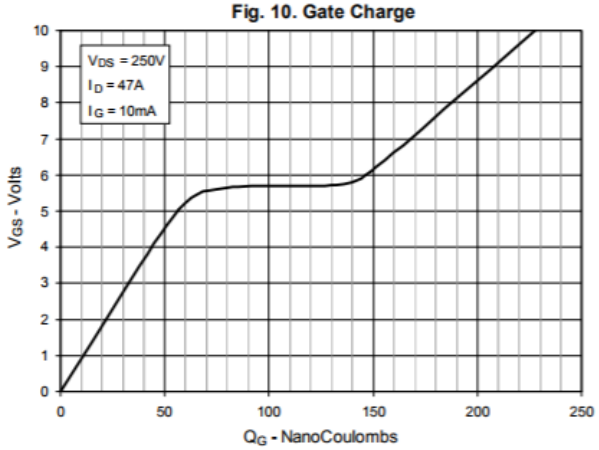


Fig. 11. Capacitance

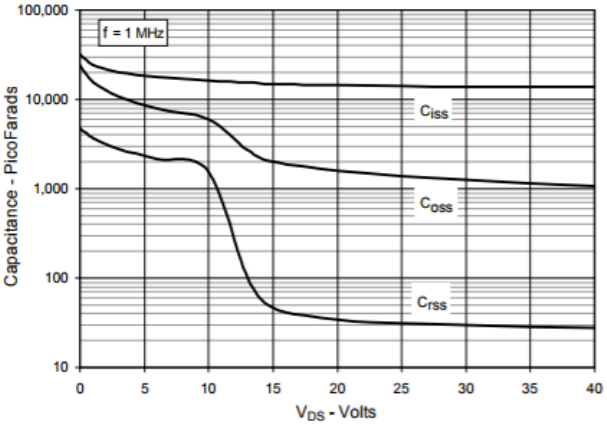


Fig. 12. Forward-Bias Safe Operating Area

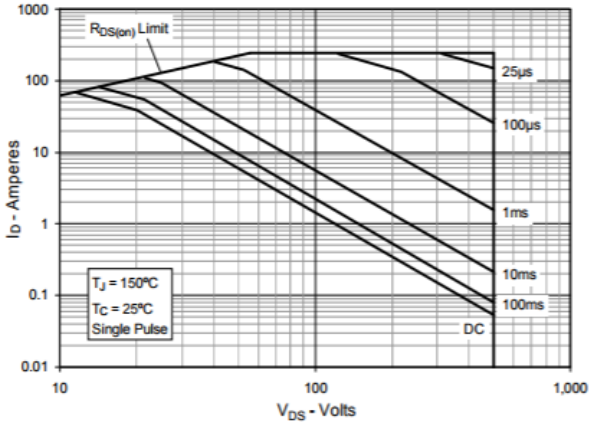


Fig. 13. Maximum Transient Thermal Impedance